AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-10. (Cancelled)

11. (Currently Amended) A non-volatile storage device comprising:

a controller;

a buffer memory; and

a nonvolatile memory,

wherein said buffer memory comprises a plurality of banks, ~~and~~

wherein an amount of data storable into said nonvolatile memory at one time is equal to an amount of data that can be stored in a plurality of said banks of said buffer memory,

wherein said controller performs control operations to receive data from outside of said nonvolatile storage device via a data terminal, to store received data to said banks of said buffer memory, and to ~~write~~transfer received data from said banks of said buffer memory to said nonvolatile memory,

wherein said controller detects whether received data has been ~~written~~transferred from each bank of said buffer memory to said nonvolatile memory, ~~and~~ performs control

operations to select, for storing further received data, one of said banks of said buffer memory that is not storing received data yet to be ~~written~~transferred to said nonvolatile memory, and performs control operations to issue a program command to said nonvolatile memory when said controller controls transfer of the amount of data to said nonvolatile memory, and

wherein said controller provides a signal, as status information, to the outside of said nonvolatile storage device when said controller detects that all of said banks of said buffer memory are storing received data yet to be ~~written~~transferred to said nonvolatile memory.

12. (Previously Presented) A nonvolatile storage device according to claim 11,

wherein a total storage size of all banks of said buffer memory equals a size of a unit of data that is written into said nonvolatile memory at a time.

13. (Currently Amended) A nonvolatile storage device according to claim 11, further comprising:

a status register including a status flag used for providing a ~~status~~state indication which indicates whether a transfer of data from said buffer memory to said nonvolatile memory has been completed, ~~and~~

wherein said status flag is set by said controller, and

wherein said controller is capable of outputting said state indication as said status information.

14. (Currently Amended) A nonvolatile storage device according to claim 13,

wherein said status flag includes a plurality of bits ~~status indication includes a plurality of flags~~ respectively corresponding to said plurality of banks of said buffer memory, and

wherein each of said ~~flags~~bits indicates whether transferring of data from the corresponding bank of said buffer memory to said nonvolatile memory has been completed.

15. (Currently Amended) A nonvolatile storage device according to claim 14, further comprising:

a first register containing information which indicates whether each of said banks of said buffer memory is storing received data, and

a second register containing information which indicates whether received data stored in each of said banks of said buffer memory has been transferred to said nonvolatile memory,

wherein said controller judges whether each of said banks of said buffer memory stores received data yet to be transferred to said nonvolatile memory, based on information contained in said first register and information contained in said second register, for setting each of said ~~of~~ bits of said status flags ~~said status indication~~.

16. (Previously Presented) A nonvolatile storage device according to claim 11, further comprising:

a register in which an address range of said nonvolatile memory is set; and

a data storage error detection circuit which detects whether data may be written to said nonvolatile memory, based on the address information that is set in said register and an amount of data that is received from the outside.

17. (Currently Amended) A nonvolatile memory apparatus comprising:

a controller having ~~a plurality of~~ memory areas; and

a nonvolatile memory,

wherein data stored in a plurality of said memory areas can be stored to said nonvolatile memory at one time,

wherein said controller is capable of receiving an arbitrary one of commands including a write command, and is adapted to perform an operation in response to a received command,

wherein in a write operation in response to receiving said write command as received command, said controller performs control operations to receive data for storing to a first memory area of said plurality of memory areas, to receive data for storing to a second memory area of said

plurality of memory areas after receipt of the data for storing to said first memory area, and to transfer data stored in said first memory area in parallel to said nonvolatile memory during receiving of the data for storing to said second memory area if said nonvolatile memory is ready to receive data,

wherein said controller is adapted to issue a program instruction to said nonvolatile memory after a transfer of data from the plurality of memory areas to said nonvolatile memory at one time, and

wherein said controller is adapted to set a signal which can be output in response to a request from outside said nonvolatile memory apparatus, when data stored in said plurality of memory areas cannot be transferred to said nonvolatile memory under a condition that said nonvolatile memory is not ready to receive data.

18. (Previously Presented) A nonvolatile memory apparatus according to Claim 17,

wherein said controller comprises a register of which a value can be output to the outside thereof, and

wherein said signal is a value of said register.

19. (Previously Presented) A nonvolatile memory apparatus according to Claim 18, further comprising a data terminal and a command terminal,

wherein said data terminal is used for receiving data corresponding to said write command, and

wherein said command terminal is used for receiving said arbitrary one of commands and is used for outputting said value of said register.